

AMENDMENTS TO THE CLAIMS:

1. (Currently Amended) A frequency divider comprising,
a first latch comprising a clock input for receiving a clock signal[[, and]] ;
a second latch comprising a latch circuit configured as a low-pass filter, the second latch
being cross-coupled to the first latch; and
wherein the second latch comprises
a differential pair of transistors including
a first pair of transistors comprising a first transistor coupled to a second transistor
- a second pair of transistors comprising a third transistor coupled to a
fourth transistor
- each transistor having a drain, a source and a gate,
[[a]] the drain of the first transistor and [[a]] the drain of the third transistor being
coupled to [[a]] the source of the second transistor and to [[a]] the source of the fourth transistor
respectively,
the gates of the second transistor and the fourth transistor receiving a signal
generated by the first latch ,
the gates of the first transistor and the third transistor being coupled to a control
signal for determining a low-pass characteristic of the second latch[[;]] , and
wherein the control signal is a DC signal.

2.-6. (Canceled)

7. (Currently Amended) A frequency divider as claimed in claim 1, wherein each latch comprises a negative resistance coupled between the drains of said second transistor and said fourth transistor and ~~between the drain of the fifth transistor and drain of the sixth transistor;~~ respectively wherein the negative resistance comprises a fifth transistor and a sixth transistor.

8. (Currently Amended) A frequency divider comprising,
a first latch comprising a clock input for receiving a clock signal[[, and]];
a second latch comprising a latch circuit configured as a low-pass filter, the second latch
being crossed-coupled to the first latch; and
wherein the second latch comprises
a differential pair of transistors including
a first transistor and a second transistor,
each transistor having a drain, a source and a gate,
- [[a]] the drain of the first transistor and the drain of the second transistor
being coupled to supply voltage (Vs) via respective resistors,
[[a]] source of the first transistor and [[a]] the source of the second
transistor being coupled to a common potential,
the gates of the first transistor and the second transistor receiving a signal
generated by the second latch,
the second latch controlled by first and second control signals, and
wherein the control signals are DC signals.

9.-12. (Canceled)

13. (Currently Amended) A frequency divider as claimed in claim 1, wherein the second latch comprises a differential pair of transistors including

a fifth transistor and a sixth transistor

each transistor having a drain, a source and a gate,

- [[a]] the drain of the fifth transistor and the drain of the sixth transistor being coupled to supply voltage via respective resistors,

[[a]] the source of the fifth transistor and [[a]] the source of the sixth transistor being coupled to a common potential,

the gates of the fifth transistor and the sixth transistor receiving a signal generated by the ~~first~~ second latch.